ABSTRACT

Voltage-dropping components are bypassed during testing of the erasing of a flash memory device thereby effectively lowering the applied erase voltage to the marginal level desired (V_{ME}). These voltage-dropping components may be a plurality of diode-connected NMOS transistors. If a plurality of diode-connected NMOS transistors are used, the voltage applied to the flash macro is reduced by $m*V_t$, where m is the number of bypassed diode connected NMOS transistors and V_t is the threshold voltage of the NMOS transistors. In normal operation, the voltage dropping components are placed in series with the charge pump, thereby returning the voltage applied to the flash macro to the normal level (V_{NE}).